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METRIC

Standard Test Method for Estimating Electromigration Median Time-To-Failure and Sigma of Integrated Circuit Metallizations [Metric][1]

This standard is issued under the fixed designation F 1260M; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method is designed to characterize the failure distribution of interconnect metallizations such as are used in microelectronic circuits and devices that fail due to electromigration under specified d-c current density and temperature stress. This test method is intended to be used only when the failure distribution can be described by a log-Normal distribution.

1.2 This test method is intended for use as a referee method between laboratories and for comparing metallization alloys and metallizations prepared in different ways. It is not intended for qualifying vendors or for determining the use-life of a metallization.

1.3 The test method is an accelerated stress test of four-terminal structures (see Guide F 1259M) where the failure criterion is either an open circuit in the test line or a prescribed percent increase in the resistance of the test structure.

1.4 This test method allows the test structures of a test chip to be stressed while still part of the wafer (or a portion thereof) or while bonded to a package and electrically accessible by means of package terminals.

1.5 This test method is not designed to characterize the metallization for failure modes involving short circuits between adjacent metallization lines or between two levels of metallization.

1.6 This test method is not intended for the case where the stress test is terminated before all parts have failed.

1.7 This test method is primarily designed to analyze complete data. An option is provided for analyzing censored data (that is, when the stress test is halted before all parts under test have failed).

1.8 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

F 1259M Guide for Design of Flat, Straight-Line Test Structures for Detecting Metallization Open-Circuit or Resistance-Increase Failure due to Electromigration [Metric][2]

F 1261M Test Method for Determining the Average Electrical Width of a Straight, Thin-Film Metal Line [Metric][2]

2.2 *Other Standards:*

EIA/JEDEC Standard 33-A— Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line[3]

EIA/JEDEC Standard 37— Lognormal Analysis of Uncensored Data, and of Singly Right-Censored Data Utilizing the Persson and Rootzen Method[3]

3. Terminology

3.1 *Definitions of Terms Specific to This Standard:*

3.1.1 *metallization*—the thin-film metallic conductor used as electrical interconnects in a microelectronic integrated circuit.

3.1.2 *test chip*—an area on a wafer containing one or more test structures that are stressed according to the test method while either is still part of the wafer or after having been separated and packaged.

3.1.3 *test line*—a straight metallization line of designed uniform width that is subjected to the current density and temperature stresses prescribed in the test method.

3.1.4 *test structure*—a passive metallization structure, with terminals to permit electrical access, that is fabricated on a semiconductor wafer by the normal procedures used to manufacture microelectronic integrated devices.

[1] This test method is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.11 on Quality and Hardness Assurance.

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[2] *Annual Book of ASTM Standards*, Vol 10.04.

[3] Available from Global Engineering, 15 Inverness Way, East Inglewood, CO 80112-5776.

4. Summary of Test Method

4.1 This test method is used to obtain sample estimates of the median-time-to-failure, t_{50}, and sigma that describe the failure distribution of metallization test lines subjected to current density and temperature stress. This involves subjecting a sample of N test structures to high current density and high ambient temperature stress, calculating the stress temperature of the metallization during the test, (which takes account of joule heating) and measuring the time to failure of each structure. The time-to-fail of the test structures is empirically described by a log-Normal distribution. The sample estimate of t_{50} is equal to the exponential of the mean of the logarithm of the time-to-fail values as follows:

$$t_{50S} = \exp \overline{ln\, t_f} \tag{1}$$

The sample estimate of sigma, s, is equal to the standard deviation of the logarithm of the time-to-fail values, scaled to remove the bias:

$$s = \left[1 + \frac{1}{4(N-1)}\right] \cdot \sqrt{\frac{\sum_{i=1}^{N} (ln\, t_{fi} - \overline{ln\, t_f})^2}{N-1}} \tag{2}$$

The failure times are plotted on a logarithm scale versus a Normal probability scale of cumulative percent failed to verify that the points plotted fall along a straight line and thereby demonstrate that they belong to a well-behaved, log-Normal distribution.

4.2 Before this test method can be implemented, a number of parameters must be selected and agreed upon between the parties to the test. These are the ambient stress temperature; the current-density stress; the temperature, T_n, to which the failure-time data shall be normalized (6.10); the failure criterion (6.3, 6.4, and 10.9.2); the number, N, of test structures to be stressed; the design width of the test lines (3.3) to be stressed (6.11); and the activation energy, E_A (6.10). Both N and s are used in 10.14 to determine the confidence limits for t_{50} and sigma.

5. Significance and Use

5.1 Electromigration is a metallization failure mechanism that is of great concern especially for the reliability assessment of very large-scale integrated (VLSI) microelectronic devices.

5.2 This accelerated stress test is used to obtain sample estimates of parameters that describe the failure distribution of the metallization at the stress conditions used in the test. These estimates are used in assessing metallization reliability and in making major decisions for the selection of metallization and processing technologies.

6. Interferences

6.1 Errors in estimating the mean current density and temperature stresses will lead to errors in the sample estimate of $t_{50}(t_{50s})$ that can be calculated by the following empirical equation:

$$t_{50s} = A(1/J)^{n} exp(E_a/kT) \tag{3}$$

where:
A = constant,
n = constant,
J = mean current density stress,
E = activation energy (see 4.2),
k = Boltzmann constant, and
T = mean stress temperature of the test lines stressed.

For typical conditions, the induced percent error in t_{50s} can be between two and three times the percent error in estimating J, and can be between 15 and 20 % if there is a 5°C error in estimating T for temperatures between 150 and 200°C.[3]

6.2 Structure-to-structure deviations from the stress means produce changes in the time-to-fail, t_f, of the individual test structures. These changes lead to increases in s and in the confidence limits for t_{50} and sigma.[3] Deviations should be kept small enough that they do not produce changes in t_f by more than 20 %.[3] This is especially important when sigma <0.4. The effect of stress deviations on t_f is calculated from (Eq 3) by substituting t_f for t_{50s}.

6.3 The effect of thermal interactions must be considered in estimating the mean stress temperature of the structures under test when more than one test structure on a test chip is stressed at a time and when joule heating is significant. These interactions are accounted for in 10.11. When the failure mode is a prescribed increase in resistance, separate corrections may be necessary if the currents to these structures have not been reduced and increases in the resistances of the failed structures during the remainder of the test produce significant increases in the power dissipation on the test chip. See 10.9.4 to avoid the need for these corrections.

6.4 The selection of a percent change in resistance as the failure criterion (4.2, 10.9.2) is required for a multilayered metallization that has one or more refractory metal layers. The value selected may affect significantly the measured activation energy, the value for n in (Eq 3), and t_{50s}.[4] The use of a large percent increase in resistance (≥30 %) as the failure criterion may lead to undesirably large variability in test results[4] and to resistance oscillations due to open circuits in all but the refractory layer, especially when testing passivated metallizations.[5]

6.5 Some abnormalities in the test line and structure, other than those detectable from a visual inspection (7.2), may be indicated by an abnormal value for $R(TS)_L$ (10.3).

6.6 The voltage limit imposed on the test structure (8.1.4) is intended to reduce the possibility of the healing of an open circuit at the moment of failure due to arcing.

6.7 It is possible, especially for passivated structures, that a test line, having failed due to an open circuit, will resume conduction spontaneously later in the test or when the stress conditions are interrupted for a period. The current to these structures shall be reduced as soon as practicable after their recovery has been detected.

6.8 The metallization to be tested must be sufficiently stable so that when it is subjected to the stress temperature of the test

[4] Ondrusek, J. C., Nishimura, A., Hoang, H. H., Sugiura, T., Blumenthal, R., Kitagawa, H., and McPherson, J. W., "Effective Kinetic Variations with Stress Duration for Multilayered Metallizations," *Proceedings International Reliability Physics Symposium*, 1988, p. 179.

[5] Maiz, J. A., and Sabi, B., "Electromigration Testing of Ti/Al-Si Metallization for Integrated Circuits," *Proceedings International Reliability Physics Symposium*, 1987, p. 145.

(but not the stress current), no significant change will occur with time in the resistance of the individual test structures or in the failure characteristics (t_{50} and sigma) of the metallization due to electromigration.

6.9 The test is applicable only for cases where t_{50} is large enough so that the resistance of the test structure under power, $R(TS)_P$, (10.8.1 and 10.8.3) can be measured before significant changes occur in the resistance or in the temperature coefficient of resistance, TCR, (10.5) of the test structures under test due to changes induced by electromigration.

6.10 The selection of the normalization temperature T_n (4.2) can affect the accuracy of the sample estimate of t_{50} to the extent that T_n is different from the mean of the metallization stress temperatures of the test structures under test (10.12) and the estimate of the activation energy (4.2 and 6.1) is inaccurate.

6.11 When comparing different metallizations of similar thicknesses by their sample estimates of t_{50}, the test structures involved in the tests shall have test lines that have the same designed width. Otherwise, the possible dependence of t_{50} on line width will interfere with such comparisons.

7. Preparatory Measurements

7.1 *Metallization Thickness*—Obtain an estimate of the metallization thickness from measurements made at five locations distributed over each wafer that is to provide test structures for the test method. This may be done after the metal deposition step with an appropriate contactless method or later on the wafer with a profilometer, for example. In the latter case, account for any consumption of the underlying dielectric or of the exposed metallization that may have occurred after the metallization deposition. Caution is also advised if a profilometer is used on passivated metallization; the deposition rate of the dielectric on the metallization may be different from the rate on other materials.

7.2 *Microscopic Inspection*—Perform a microscopic inspection of the test structures to be stressed. Reject structures intended for the test which have test lines that are discontinuous or have other abnormal physical features that can be observed. If structures are packaged, ensure that any package wire bonds electrically connecting the chip bonding pads to the package terminals do not touch other wire bonds or other parts of the test chip or package.

7.3 *Metallization Line Width*—Obtain an estimate of the electrical width of the test line.

7.3.1 The metallization line width shall be measured electrically using a special test structure (see Test Method F 1261). The test line of this structure shall be parallel to the test line of the structure to be tested as well as have the same designed line width and shall have the same local design features that can affect the width of the processed line.

7.3.2 If the stress test is to be performed on packaged test chips, the estimate of the line width shall be obtained from measurements of the special test structure that is included on the bonded chip and electrically accessible by means of the package terminals.

7.3.3 If the stress test is to be conducted on the wafer, the estimate of the electrical line width shall be obtained from measurements of the special test structure that is located close enough to the electromigration test structures to be stressed so that no significant change in line width over the wafer is expected.

7.4 *Metallization Cross-Sectional Area*—Calculate an average value for the cross-sectional area of the test lines to be stressed on a test chip by taking the product of the metallization thickness obtained from 7.1 and the line width from 7.3. An approximate estimate for the cross-sectional area of the test line may be obtained by an electrical method that involves the measurement of the resistance of a special, nearby test structure (see Test Method F 1261M) at two temperatures when the primary electrical conduction of the line is by means of an aluminum alloy. Ignoring deviations from Matthiessen's rule[6] and the effects of thermal expansion, an estimate of the cross-sectional area, A, of the metal line can be obtained from the following equation:

$$A = \frac{L \times 0.01146 \cdot 10^{-6}}{dR/dT} \, (\text{cm}^2) \tag{4}$$

where:

L = length of the line in the special test structure, and
dR/dT = slope of the resistance of the line with temperature.[6]

Corrections have to be made to this estimate when making measurements of layered metallizations where the other layers are of materials with much higher electrical resistivity.

8. Test Circuit

8.1 The test circuit used shall have the following capabilities:

8.1.1 The current through each test structure shall be individually adjustable to the current necessary to attain the desired current density stress and be maintained constant during the stress test to within ±1 % of that current or 25 µA, whichever is greater (see 6.1 and 6.2).

8.1.2 The display resolution of the voltage if used to determine the current through a test structure shall be equivalent to 0.1 % of the intended stress current or 10 µV, whichever is greater (see section 6.1.).

8.1.3 The display resolution of the voltage between the voltage taps of each test structure shall be equal to at least 0.1 % of the display voltage before and during the stress test when used to make resistance measurements (6.1.). When used to monitor for open-circuit failure, the display resolution of the voltage shall be at least 5 % of the display voltage.

8.1.4 The maximum voltage applied across the test structure during the stress test, and including the time of failure, shall be less than that voltage where an open-circuit failure can self heal (see section 6.6.). A suggested voltage limit is 15 V.

9. High-Temperature Stress Environment

9.1 *For a Packaged Test Chip*—A sensor with a display resolution of at least 0.5°C shall be used to measure the

[6] Schafft, H. A., Mayo, S., Jones, S. N., and Suehle, J. S., "An Electrical Method for Determining the Thickness of Metal Films and the Cross-Sectional Area of Metal Lines," *IRW Final Report, IEEE Catalog Number 94TH0654-4*, 1995, pp. 5–11.

temperature of a heat sink in intimate thermal contact with the package. The point of measurement shall be within a distance *l* from the perpendicular axis of the bonded chip, where, *l*, is the length of one side of the chip.

9.2 *For Test Samples on a Wafer or Some Portion Thereof*—A sensor with a display resolution of at least 0.5°C shall be used to indicate the temperature of the heated surface used to produce the high temperature stress. This heated surface shall be in intimate thermal contact with the underside of the substrate. The difference between the temperature of the wafer top surface near where the structures to be tested are located and the temperature indicated by the sensor used to measure the heated surface shall be known within ±2°C (see 6.1).

9.3 The oven for the packaged devices or the heated surface for the wafer shall be able to maintain the high temperature environmental stress constant to within ±2°C for temperatures up to 200°C and within ±3°C for higher temperatures (see 6.1).

10. Procedure

10.1 Install test parts.

10.1.1 If packaged test samples are to be used, install packages in oven sockets fitted with heat sinks having a means for measuring the temperature near where the test chip is located in the package (9.1 and 9.3). Use a heat-conducting compound at the interface between package and heat sink to promote good heat transfer at the interface.

NOTE 1—It is suggested that the temperature of the heat sink be measured by a thermocouple inserted into a hole that has been drilled from one end of the heat sink to a point near where the test chip would be located.

10.1.2 If the test structures to be tested are on a wafer or a part thereof, employ a pressure-differential method to hold the substrate to the surface that is to be heated to the hightemperature stress of the test (9.2 and 9.3).

10.2 Determine the thermal response time of the test system in the manner described in Annex A1 if packaged parts are to be used and if joule heating will be such that the mean value for $T(TS)_P - T(TS)_o$ will be greater than 2°C (see 10.7.1 and 10.8.4).

NOTE 2—The procedure in 10.2 can be performed earlier with an equivalent physical configuration and with equivalent packaged parts.

10.3 Measure the resistance, $R(TS)_L$, of each test structure at room temperature.

10.3.1 Ensure that the test structures are in thermal equilibrium with the local environment containing the sensors used to monitor the temperature.

10.3.2 Determine the temperature of the test structures, $T(TS)_L$.

10.3.2.1 If packaged samples are to be tested, measure the temperature of each package heat sink to determine the temperature of the structures in each package.

10.3.2.2 If the structures to be tested are on a wafer, determine the temperature of the top surface of the hot stage near where the structures would be located.

10.3.3 Measure the resistance $R(TS)_L$ of each test structure at temperature $T(TS)_L$ using a current that is sufficiently small to produce negligible joule heating. To determine if joule heating is negligible, halve the current and remeasure the resistance. If no significant change in resistance is noted by doing this, the original current used is acceptable.

10.4 Measure the resistance, $R(TS)_H$, of each test structure at the ambient stress temperature.

10.4.1 Elevate the temperature of the oven or heating stage to the ambient stress temperature (4.2).

10.4.2 Ensure that the high-temperature ambient has reached an equilibrium condition.

10.4.3 Determine the temperature of the test structure, $T(TS)_H$.

10.4.3.1 If packaged parts are to be tested, measure the temperature of the heat sink of each package to determine the temperature of the structures in each package.

10.4.3.2 If the structures to be tested are on a wafer, determine the temperature of the top surface of the hot stage near where the structures would be located.

10.4.4 Measure the resistance of each test structure at the elevated temperature, $R(TS)_H$, using probe currents approximately equal to those used in 10.3.3.

10.5 Calculate the temperature coefficient of resistance, $TCR(T)$, for the test structures to be stressed, referenced to temperature $T(TS)_L$. See EIA/JEDEC Standard 33-A for measurement interferences and precision of measurement method.

10.5.1 Calculate either the $TCR(T(TS)_L)$ of each test structure or of a representative number of structures to obtain an estimated mean value for the structures to be stressed.

10.5.2 Use the following equation to calculate $TCR(T(TS)_L)$:

$$TCR(T(TS)_L) = \frac{R(TS)_H - R(TS)_L}{R(TS)_L \cdot \{T(TS)_H - T(TS)_L\}} \quad (5)$$

10.6 Calculate the current in each test structure necessary to attain the desired current-density stress by taking the product of the current density selected (4.2) for the test and the cross-sectional area determined from 7.4.

10.7 Initiate stress test.

10.7.1 Monitor the temperature of the test structures as directed in 10.4.3 for a period sufficiently longer than the cyclic temperature variations of the high-temperature environment to obtain a mean temperature, $T(TS)_o$, for the test structures on the test chip.

10.7.2 Set timer to zero and increase the current through each test structure to the level determined in 10.6.

NOTE 3—The test structures of the test sample may be placed on test all at the same time, in groupings by test chip, or individually (6.8).

10.8 Measure the initial metallization stress temperature, $T(TS)_P$.

10.8.1 Measure the resistance of each test structure, $R(TS)_P$, at a time after the stress current has been applied that is approximately equal either to one thermal response time of the system (if its determination was required in 10.2) or to 1 min (see 6.9).

10.8.2 If more than one structure on the test chip is stressed simultaneously and if joule heating will be such that $T(TS)_P - T(TS)_o$ (10.7.1 and 10.8.4) will be greater than 2°C, calculate the average power, P, dissipated by the structures under test in 10.8.1.

10.8.3 If, in addition to conditions of 10.8.2, packaged samples are used, measure the temperature of each heat sink, $T(HS)_P$, at the time $R(TS)_P$ is determined.

10.8.4 Calculate the stress temperature of each test structure using the following equation:

$$T(TS)_P = T(TS)_o + \frac{R(TS)_P - R(TS)_H}{R(TS)_L \cdot TCR(T(TS)_L)} \tag{6}$$

10.9 Determine time-to-fail of each test structure.

10.9.1 Monitor the voltage across each test structure at intervals that are less than 5 % of the test time or 15 min, whichever is larger.

10.9.2 Determine the time at which the voltage across the test structure indicates that the structure has failed according to the failure criterion selected: an open circuit or a preselected percent increase in the resistance of the test structure. For the latter criterion, the percent increase in resistance selected shall be no greater than 30 % (see 6.4.).

10.9.3 The time-to-fail, t_f, is calculated as follows:

$$t_f = \sqrt{t_1 t_2} \tag{7}$$

where:

t_2 = time recorded in 10.9.2, and
t_1 = time when the test structure was previously last monitored (10.9.1).

10.9.4 If the failure criterion is a percent increase in resistance, reduce the current to the failed structure to a negligible value as soon as practicable after failure has been detected.

10.9.5 Proceed to 10.11 if only one test structure on the test chip is stressed at a time (6.8) or if the $T(TS)_P - T(TS)_o$ values for the structures under test are <2°C.

10.10 Calculate the value to be used for the thermal resistance of the test system in the manner described in Annex A2 if more than one test structure in a test chip is to be stressed at a time and the $T(TS)_P - T(TS)_o$ values are >2°C.

NOTE 4—The calculation of the thermal resistance (if required) is performed earlier with an equivalent physical configuration and with a representative sample of test chips on a wafer or of packaged test chips, according to which are used in this test method.

10.11 Estimate the mean stress temperature, T_s, of each test structure under test in each of the test chips involved in this test method.

10.11.1 If either of the conditions in 10.9.5 apply, equate T_s to the value obtained for $T(TS)_P$ in 10.8.4 and proceed to 10.12.

10.11.2 If more than one structure of the test chip is stressed at a time on a wafer, ΔT is used in 10.11.4 and defined as follows:

$$\Delta T = P \cdot R_{\theta(W-A)} \tag{8}$$

where:

P = average power dissipated by the test structures on the test chip as determined in 10.8.2, and
$R_{\theta(W-A)}$ = that which was determined in Annex A2.

10.11.3 If more than one structure is stressed at a time on a packaged chip, ΔT is used in 10.11.4, and defined as follows:

$$\Delta T = P \cdot \{R_{\theta(C-HS)} + R_{\theta(HS-A)}\} \tag{9}$$

where:

P = average power dissipated by the test structures in the package as determined in 10.8.2,
$R_{\theta(C-HS)}$ = that which was determined in Annex A2, and
$R_{\theta(HS-A)}$ = that which was determined in Annex A2.

10.11.4 Calculate T_s for each of the N test structures on the test chip to fail consecutively in times t_{f1}, t_{f2}, ... t_{fN}, determined in 10.9.3, by using the following equations:

$$T_s(1) = T(HS)_P, \text{ (see 10.8.3), and for } 1 < M \leq N$$

$$T_s(M) = T(M)_P - \Delta T \cdot \left[(M-1) - \frac{\sum_{i=1}^{M-1} t_i}{t_M} \right] \tag{10}$$

using M as the index which can represent any number from 2 to N in generating expressions for $T_s(M)$ *where* M = 2, 3, ... to N, and where: ΔT equals that which is taken from 10.11.2 or 10.11.3. If the failure criterion is a percent increase in resistance, use the times at which the current to the failed structures were reduced to near zero (10.9.4) if they differ significantly from the actual failure times.

10.11.5 Repeat 10.11.4 for as many test chips as are involved in the test.

10.12 Calculate the mean stress temperature T_m and the standard deviation $SD(T_m)$ of the test-structure stress temperatures determined in 10.11 (see 11.1.9 and 11.1.10).

10.13 If the stress test was terminated before all parts had failed, proceed to 10.18. Otherwise, calculate the sample estimates of the median time-to-failure, t_{50}, and of sigma, t_{50s}, and s, respectively, and their confidence limits.

10.13.1 Calculate the mean, $\bar{Y}$, of the ln (t_f) values obtained from 10.9.3 and the standard deviation of these values.

NOTE 5—The procedure for determining the sample estimates of median time-to-failure and sigma is intended for use only with data that includes the failure times of all of the parts that were placed on test. If the procedure is used for incomplete (censored) data, the sample estimates will be biased low.

10.13.2 The sample estimate of t_{50} is equal to the exponential of the mean calculated in 10.13.1, as follows:

$$t_{50} = \exp \bar{Y} \tag{11}$$

10.13.3 The sample estimate of sigma, s, is equal to the standard deviation determined in 10.13.1 multiplied by 1 + 1/4(N − 1), where N is the sample size. [7]

10.14 Calculate 90 % confidence limits for t_{50} and sigma.

10.14.1 The 90 % confidence limits for t_{50} are as follows:

$$t_{50s} \exp[\pm t(0.95; N-1) \cdot s/\sqrt{N}] \tag{12}$$

where:

$t(0.95; N-1)$ = 95th percentile of the t distribution for $N-1$ df,
N = number of samples, and
s = sample estimate of sigma (10.13.3).

10.14.2 The 90 % confidence limits for sigma are:

$$s\sqrt{\frac{N-1}{x^2(0.95; N-1)}} \text{ and } s\sqrt{\frac{N-1}{x^2(0.05; N-1)}} \tag{13}$$

[7] Dixon, W. J., and Massey, F. J., Jr., *Introduction to Statistical Analysis*, McGraw-Hill Book Co., 1983, p. 145.

where:

s	=	sample estimate of sigma (10.13.3),
$x^2(0.95;\ N-1)$	=	95th percentile of the x^2 distribution with $N - 1$ df, and
$x^2(0.05;\ N-1)$	=	5th percentile of the x^2 distribution with $N - 1$ df.

10.15 Plot the t_f data.

10.15.1 Calculate the cumulative percent failure of each test structure in units of $1/(N+1)$, where N is the number of structures stressed in the test.

10.15.2 Plot the t_f failure times determined in 10.9.3 on a logarithm scale versus a Normal probability scale of cumulative percent failed to verify that the points fall along a straight line and thereby demonstrate that the data belong to a well-behaved, log-Normal distribution.

10.16 Calculate the sample estimate of t_{50}, normalized to stress temperature T_n (4.2) by using the following equation:

$$t_{50sn} = t_{50s} \exp \frac{E_a}{k_n} \left(\frac{1}{T_n} - \frac{1}{T_m} \right) \quad (14)$$

where:

T_m	=	value determined in 10.12,
$E_a\ (eV)$	=	activation energy, and
k_n	=	8.617×10^{-5} eV/K (see 6.10.).

10.17 Calculate the 90 % confidence limits for $t_{50_{sn}}$ by multiplying the limits calculated in 10.14.1 by $t_{50_{sn}}/t_{50_s}$.

10.18 When the failure-time data is incomplete because the stress test was halted before all parts under test had failed, calculate the unbiased sample estimates of the median time-to-failure, t_{50}, and of sigma, t_{50s}, and s, respectively, using EIA/JEDEC Standard 37 for right-censored data.

10.19 Calculate the sample estimates of t_{50}, normalized to stress temperature T_n (4.2) by using Eq 11.

11. Report

11.1 Report, as a minimum, the following information:

11.1.1 Identification of operator(s) and dates of test,

11.1.2 Equipment used,

11.1.3 Metallization tested,

11.1.4 Means of the test-line width, thickness, and length (1.3, 7.3, 7.1),

11.1.5 Mean and range of $R(TS)_L$ values (10.3),

11.1.6 Mean and range of the $T(TS)_P - T(TS)_o$ values (10.7, 10.8),

11.1.7 Current-density stress (4.2),

11.1.8 Ambient stress temperature (10.4.3),

11.1.9 Mean of the test-structure stress temperatures, T_m (10.12),

11.1.10 Standard deviation of the test-structure stress temperatures $SD(T_m)$ (10.12),

11.1.11 Normalized stress temperature, T_n (4.2),

11.1.12 Number of test structures stressed, N (4.2),

11.1.13 Failure criterion (4.2),

11.1.14 Sample estimate of the median-time-to-failure normalized to T_n, t_{50sn}(10.16 or 10.19),

11.1.15 Sample estimate of sigma, s (10.13.3 or 10.18),

11.1.16 The 90 % confidence limits for t_{50_n} and for sigma (10.14.2 and 10.17), for complete data, and

11.1.17 Plot of normalized time-to-fail data on probability by logarithmic graph paper (10.15).

12. Keywords

12.1 electromigration; electromigration metallization; integrated circuit; microelectronics; open circuit; resistance increase; time-to-failure

ANNEXES

(Mandatory Information)

A1. THERMAL RESPONSE TIME DETERMINATION

A1.1 With a representative test package installed, elevate the oven temperature so that it is approximately 50 % of the anticipated ambient stress temperature to be used. The thermal response time of a test structure while part of a wafer mounted on a hot stage will be much less than a minute and does not need to be measured.

A1.2 Select a current for the test structure on the test chip to be stressed so that joule heating raises the temperature of the test metallization by approximately 10°C.

A1.3 Monitor the voltage across the test structure at least every minute.

A1.4 While monitoring the test-structure voltage, switch on the current (see A1.2).

A1.5 Continue monitoring the test structure voltage until no further increase in voltage is noted.

A1.6 The thermal response time of the test system is the time required for the test structure voltage to attain a constant value.

A2. THERMAL RESISTANCE CALCULATIONS

A2.1 Perform procedures in 10.1 through 10.5 with a representative sample of test chips. The test chips shall be packaged or part of a wafer, depending on which will be used in the test method.

A2.2 If the test chips are on a wafer, calculate the thermal resistance between the wafer and the heated surface for each test chip of the representative sample.

A2.2.1 Select a current, I_t, that will produce a conveniently measurable temperature rise in a test structure due to joule heating.

A2.2.2 Subject one test structure in the test chip to current I_t only long enough to measure the structure's resistance approximately 1 min after the application of the current. Call this resistance $R(TS)_{PS}$.

A2.2.3 Calculate the temperature increase of the test structure due to joule heating, $\Delta T_W(s)$, by using the following equation:

$$\Delta T_W(s) = \frac{R(TS)_{PS} - R(TS)_H}{R(TS)_L \cdot TCR} \quad (A2.1)$$

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where the values for $R(TS)_H$, $R(TS)_L$, and TCR are obtained from A2.1.

A2.2.4 Subject all of the structures in the test chip to current I_t only long enough to measure the resistance of the test structure used in A2.2.2 approximately 1 min after the current has been applied. Call this resistance $R(TS)_{Pa}$.

A2.2.5 Calculate the temperature increase of the test structure due to joule heating, $\Delta T_W(a)$, by using the following equation:

$$\Delta T_W(a) = \frac{R(TS)_{Pa} - R(TS)_H}{R(TS)_L \cdot TCR} \quad (A2.2)$$

A2.2.6 Calculate the mean power, P_W, dissipated by the test structures stressed in A2.2.4.

A2.2.7 Calculate the thermal resistance between the wafer and the heated surface using the following equation:

$$R_{\theta(W-A)} = \frac{\Delta T_W(a) - \Delta T_W(s)}{(M-1) \cdot P_W} \quad (A2.3)$$

where M is the number of structures in the test chip that were stressed simultaneously in A2.2.4.

A2.3 If packaged test chips are to be tested, calculate the thermal resistance between the chip and the heat sink, and between the heat sink and the high-temperature environment for each package of the representative sample.

A2.3.1 Select a current, I_t, that will produce a conveniently measurable temperature rise in a test structure due to joule heating.

A2.3.2 Subject one test structure in the test chip to current I_t only long enough to measure the structure's resistance approximately one thermal response time (10.2) after the application of the current. Call this resistance $R(TS)_{PS}$.

A2.3.3 Calculate the temperature increase of the test structure due to joule heating, $\Delta T_{PKG}(s)$, by using the following equation:

$$\Delta T_{PKG}(s) = \frac{R(TS)_{PS} - R(TS)_H}{R(TS)_L \cdot TCR} \quad (A2.4)$$

where the values for $R(TS)_H$, $R(TS)_L$, and TCR are obtained from A2.1.

A2.3.4 Subject all of the structures in the test chip to current I_t. After a time approximately equal to one thermal response time (10.2), measure the resistance, $R(TS)_{Pa}$, of the test structure used in A2.3.2 and measure the package heat sink temperature, $T(HS)_P$. Then turn off the current to the structures.

A2.3.5 Calculate the temperature increase of the test structure due to joule heating, $\Delta T_{PKG}(a)$, by using the following equation:

$$\Delta T_{PKG}(a) = \frac{R(TS)_{Pa} - R(TS)_H}{R(TS)_L \cdot TCR} \quad (A2.5)$$

A2.3.6 Calculate the mean power, P_{PKG}, dissipated by the test structures stressed in A2.3.4.

A2.3.7 Calculate the thermal resistance between the chip and the heat sink using the following equation:

$$R_{\theta(C-HS)} = \frac{\Delta T_{PKG}(a) - \Delta T_{PKG}(s)}{(M-1) \cdot P_{PKG}} \quad (A2.6)$$

where M is the number of structures in the test chip that were stressed in A2.3.4.

A2.3.8 Calculate the thermal resistance between the heat sink and the high-temperature ambient using the following equation:

$$R_{\theta(HS-A)} = \frac{T(HS)_P - T(TS)_H}{M \cdot P_{PKG}} \quad (A2.7)$$

where $T(HS)_P$ was measured in A2.3.4 and $T(TS)_H$ was determined in A2.1.